RESPONSE under 37 C.F.R. § 1.111
U.S. Appln. No. 10/003,170

## REMARKS

Claims 1, 3-4, 6-10, 12 and 16-21 are all the claims pending in the present application and stand rejected. Reconsideration and allowance of all pending claims are respectfully requested in view of the following remarks.

**PREVIOUS RESPONSE.**

The present Office Action no longer asserts any of the previous rejections of record and thus, although it is not expressly indicated, it is presumed Applicant's previous response has overcome all prior art rejections of record.

**CLAIM REJECTIONS.**

**35 U.S.C. § 103**

Claims 1, 3-4, 6-10, 12 and 16-21 are rejected under 35 U.S.C. § 103(a) as being unpatentable over US 5,140,681 to Uchiyama et al. ("Uchiyama") in view of US 6,493,800 to Blumrich or in view of this combination in further view of US Application 22022/0184445 U.S. to Cherabuddi or US 4,930,066 to Yokota. Applicant respectfully traverses these rejections for the following reasons.

All rejections of record rely on the main memory 5 of Uchiyama to be modified with Blumrich's dymamic altering of a portion of cache. Applicant respectfully submits the present rejections are flawed because (i) there is no proper motivation to combine these references as proposed; and (ii) even when combining the teachings of Uchiyama with Blumrich, the limitations present in Applicant's independent claims are not disclosed or suggested.

(i) THERE IS NO PROPER MOTIVATION TO COMBINE REFERENCES

Uchiyama relates to subdividing a main memory 5 (see Figs. 2 and 5) into a shared region. The main memory 5 is subdivided into a shared region to be subjected to a write access from a plurality of processors. Main memory 5 includes a copy-back region 61 dedicated to processor 1, a copy-back region 62 dedicated to processor 2 and shared write-through regions 60 and 63 which may be written to by either processor 1 or 2. (Col. 5, ll 15-28). Processors 1 and 2 have caches 3 and 4 (Fig. 2) respectively associate therewith, which are in turn connected to a main memory bus 7 so as to be linked to main memory 5. (Col. 3, ll. 46-51). Cashes 3 and 4 include address and data arrays 10-13 which are used to temporarily store data of main memory 5. (Col. 3, ll. 62-65).

Blumrich discloses a dynamically partitioned cashe memory 70 (Fig. 7) which is shared among a plurality of entities (e.g., processors). Blumrich teaches that because caches are comprised of small amount of fast storage, they are expensive and it is advantageous to share. (Col. 1, ll. 47-49). However, independently operating processors can generate the same addresses which may actually refersto different memory locations. This may result in destructive collision in a shared cache. (Col. 2, ll. 5-12). Further, because processors frequently use different amounts of cache and a minimum amount may be required for a processor to achieve desired performance, Blumrich discloses a system that includes a cache segregator and a specially addressing format to dynamically vary the amount a cache that may be reserved for each processor.

The Office Action alleges it would be obvious to adapt Uchiyama main memory 5 to have the dynamic adjustment characteristics disclosed by Blumrich to provide "improved performance by providing efficient memory usage based on operating conditions of the system." Respectfully, Applicant notes that Uchiyama has its own cache system 12, 13 (Fig. 2). Further, there is no disclosure by Blumrich which would indicate that modification of a main memory

(e.g., Uchiyama memory 5) to by dynamically partitionable would have any advantages whatsoever. Further, based on the addressing mentioned in Uchiyama, it is assumed portions of memory 5 are of a fixed size and thus Uchiyama certainly does not provide any motivation for making dynamically altering the size of copy-back regions 61 and 62.

Respectfully, the motivation to modify the Uchiyama main memory partitions with the dynamic cache techniques disclosed by Blumrich are not derived from the references themselves and it appears to be merely speculation by the Examiner as to any advantages which may be obtained from doing so. In actuality, the motivation to combine the references as suggested in the Office Action appear to be nothing more than a piecemeal attempt to reconstruct Applicant's claims based on impermissible hindsight of Applicant's disclosure. Such motivation is improper and does not establish *prima facie* obviousness.

(ii) THE PROPOSED COMBINATION FAILS TO TEACH OR SUGGEST THE LIMITATIONS OF APPLICANT'S CLAIMS

Even assuming it would be proper to combine the teachings of Uchiyama with Blumrich (*arguendo*), Applicant respectfully submits the resulting combination still fails to teach or suggest the limitations of Applicant's independent claims. For example, claim 1 recites:

> *An apparatus comprising:*
> *an individual memory device including a memory array having a first portion and a second portion, the first portion of the memory array being different than the second portion of the memory array, wherein the memory array is adapted such that the first portion of the memory array is accessible only by a first processor and the second portion of the memory array is accessible only by a second processor, wherein the memory array further comprises a third portion that is different than the first portion and the second portion, the third portion of the memory array accessible by both the first processor and the second processor, and wherein the memory array is further adapted to dynamically alter a size of the first portion and the second portion of the memory array depending on an operational load of the first processor or the second processor.*

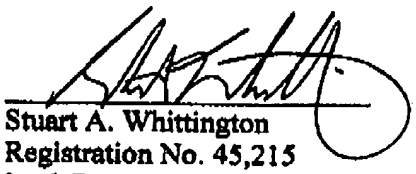
Even when combining the teachings of Uchiyama with those of Blumrich, Applicant respectfully submits that the resulting combination would merely be a system having the fixed partitioned main memory 5 of Uchiyama and a cache memory 3, 4 that may be shared and dynamically adjusted as disclosed by Blumrich. In other words, the skilled artisan considering the teachings of Blumrich, would not modify the Uchiyama main memory 5 as alleged in the Office Action, but rather would modify the cache architecture/layout of Uchiyama caches 3, 4. Accordingly, even when combining references, the resultant combination would not disclose or suggest a memory device having first and second processor-exclusive portions which may be dynamically adjusted and a third shared portion accessible by both processors. The secondary references Cherabuddi and Yakota also fail to make up for this deficiency of the Uchiyama/ Blumrich combination and thus *prima facie* obviousness of Applicant's independent claims has not been established. Applicant's dependent claims, by virtue of their dependency, are also believed to be patentable over the cited prior art for at least for the same reasons.

Since Uchiyama, Blumrich, Cherabuddi and/or Yakota, taken alone or in any combination, fail to disclose or suggest all the features of Applicant's claims, reconsideration and withdrawal of all 103 rejections are respectfully requested.

**CONCLUSION.**

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below. Applicant hereby petitions for any extension of time which may be required to maintain the pendency of this case, and any required fee or deficiency thereof, except for the Issue Fee, is to be charged to **Deposit Account # 50-0221.**

Respectfully submitted,



Stuart A. Whittington
Registration No. 45,215
Intel Corporation
(480) 715-3895

c/o
Blakely, Sokoloff, Taylor & Zafman, LLP
12400 Wilshire Blvd., Seventh Floor
Los Angeles, CA. 90025-1026
(503) 264-0967

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